Pixel FE Electronics Issues

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Lessons from recent DMILL submission, and next steps:

- Major effort devoted to FE-D front-end chip. Several design problems found, but now fairly well characterized and agree with simulation results. Several serious problems remain, which we attribute to fabrication.
- Other devices in run basically work, with exception of DORIC-p.
- Near future plans include processing 4 backup wafers to investigate yield problems, followed by a new engineering run with all known errors fixed.

Status of work on Honeywell SOI version of FE chip

- Layouts of some blocks done. Indications are good for 300μ B-layer pixel size.

Deep sub-micron status

- Short update (not much new...)

Summary of FE-D Errors and Changes for FE-D2

Analog:

- VTH amplifier layout error easily fixed for FE-D2 in layout.
- Continuing to study analog performance. In particular, studies of bump-bonded assemblies could suggest additional aspects of front-end to improve. Presently, main systematic is right/left TOT variation (not understood).
- Adjust VCCD/VTH DAC range to maximize threshold control.
- Minor modification to chopper to allow improved monitoring/calibration.
- Minor modification to Current DAC LSBs to improve linearity.
- Add injection/feedback capacitor array to allow absolute calibration of internal caps.

Integration:

- Basic problem: Missing or mis-sized buffers in several critical locations. Clearly, we are reviewing buffer sizing in detail for the entire chip. Have agreed on procedure to try to systematically find all remaining buffering problems in chip.
- Several buffers for control logic were undersized, so some commands must be “slowed down” in software. Easy to increase sizing to correct values.
- Two critical clocks (XCK, CLK1/CLK2) not distributed with adequate buffering. Simulations and measurements indicate these errors are dangerous but not fatal

in pre-rad chip operation. XCK buffer size will be increased, CLK1/CLK2 buffering will be distributed from 18 blocks at bottom-of-column for FE-D2.

- Missing buffer in serial output stream. This causes data corruption unless VDD supply increased to maximum value permitted by process (about 5V). Have verified using FIB surgery that bringing this signal out directly using an active probe allows us to operate the full chip correctly with VDD = 3.0V. Buffer can easily be added at serializer output for FE-D2.
- Missing connection to one address pad. Mistake not caught due to design kit error. Easily fixed for FE-D2.
- Modify self-trigger circuit to support new “arming” protocol so that operation with PLL and MCC will work properly. Simple modification to logic, and not critical for chip operation so risk is low.

Digital Readout:

- Missing column masking on Buffer Overflow OR tree. Simple logic change, already implemented in FE-D2.
- Will continue studies of all aspects of digital readout to look for other problems. In particular, have not performed complete tests of EOC buffers, searching in particular for any indications of “leaky” transistors (two dynamic comparators used). Also interesting from yield point of view (216 buffers per chip).

Serious problems not attributed to design errors:

- **Pixel Register Yield:** very poor yield observed for 2880 bit register in pixel matrix used for individual pixel control. Note this register is “quasi-static” in order to reduce transistor count. Extensive analysis examined behavior of defective pixels as a function of VDD, clock frequency and duty cycle, and made detailed comparisons with simulations. Yield is about 0.3 for 3mm^2 of circuitry. Very good consistency with a model in which a particular PMOS has a defect rate of 1:5000, with the defect being a drain-source resistance of several megohms.
- **Digital Readout Failures:** There are many defective pixels which cause peculiar digital “oscillations” in the column-pair readout circuitry. Detailed studies of behavior, and comparisons with simulations, suggest a problem with a defective NMOS, also with a drain-source resistance of several megohms. Here, the defect rate is much higher, about 1:200.
- **Digital Power Anomalies:** Significant number of chips with anomalous DC digital power consumption, which otherwise seem to work correctly.
- Work is continuing to develop clearer evidence for our understanding of these problems (both Bonn and LBL). This includes more aggressive surgery to isolate individual devices in bad pixels, and characterize the faults precisely (make transistor curves and show decaying signals on dynamic nodes). This should take several weeks to complete.

What did we learn in Nantes ?

- Spent a full day with large number of technical experts, and clarified many small details, including process monitoring, maximum voltages and lifetime issues, standard cell library and design kit issues.
- For MCC-D, the support for the standard cell library does not seem quite adequate (need post-rad corner models for cells).
- Lengthy discussions on yield prospects (modest improvements expected), and presentations of results for other ATLAS DMILL chips (largely good). Recently LArg also had low yield experience involving leaky transistors, but experts claim there is no relationship...
- Spent significant time discussing specific FE-D problems. No particular break-throughs, but definite interest in working with us to gain insight.
- Next steps for TEMIC include: physical analysis of some defective chips (Bonn to provide samples with coordinate information on defects), and immediate processing of four backup wafers on a fast timescale. After internal discussion, TEMIC experts proposed no poly mask changes. We will provide new GDS for metal masks, allowing us to make minor modifications.
- Next steps for us include: more detailed attempts to prove our failure hypotheses, and quick study of temperature dependence of our shift register and readout yield problems (real leakage could have large T dependence).

Next Steps for FE-D

- Work on modifications for backup wafer run. The M1 and M2 masks are needed shortly and will implement debugging aids and minor fixes. Our list includes: cut VTH Amplifier output trace, fix GA2 pad, provide access to critical M1 dynamic nodes by cutting holes in M2, and try to eliminate minor features of layout near defective devices that could conceivably have an influence on yield.
- So far, neither we nor TEMIC are doing anything significant which would make this run different than the previous FE-D run. This run should take 4-6 weeks to return, and we will most likely wait for these wafers before sending in FE-D2.
- Complete presently known modifications to FE-D design database to make FE-D2. List of changes is quite modest (but critical !).
- Continue intensive simulation and verification work on FE-D2 database.
- Do PS irradiations on PM bars and Analog Test chips to validate performance of individual devices and analog portions of FE-D under irradiation.
- Actual submission date for FE-D2 will depend on factors above, but should be as early as possible (during March) to allow us to complete serious evaluation this Summer (PS and other irradiations, single-chip and module assemblies, testbeams, etc.). Several activities may not be completed by submission date.

Reviews:

- We will probably need to undergo a “lightweight review” of what we have learned from FE-D and what we propose to change in FE-D2. Not clear when and where this will take place, as returning again to CERN in March is not attractive.
- In general, we have deviated significantly from ATLAS procedures for electronics reviews. We have had only a single preliminary review six months before submitting FE-D, where reviewers felt documentation was inadequate. Have been resisting this process, because we do not have enough resources to produce necessary documentation. This is not viewed positively by others.
- We will need to do better for FE-H. In addition, almost certainly, we must pass an FDR for FE-D before any submissions beyond FE-D2. This requires assembling a decent review team, and bringing them up to speed on our design and results. In the most optimistic scenario, this could occur this Fall, assuming all work between now and then has a successful outcome.

We desperately lack adequate manpower for our electronics developments...

Summary of MCC-D and VDC-p

MCC in DMILL:

- Present MCC-D0 was a very much simplified prototype. It appears to work well, but it has not been exhaustively tested yet. Irradiation studies are critical to see whether DMILL will really work for pixels (serious concern for lifetime dose).
- Next step is the full MCC in DMILL. The specifications for this chip are progressing well, and documentation is appearing. Die size for this chip reamins an issue. The prototyping of MCC-D will probably require a dedicated engineering run (with a new version of the opto-chips ?). Still too early to make a serious estimate of the submission date, but it is not soon (late Summer ?).

VDC-p:

- Initial testing looks promising. Seems to meet speed requirements. However, a great deal of systematic testing remains. This will be largely carried out by Wuppertal. Shortage of DORICs makes this more challenging...
- Irradiation studies are planned for April, involving collaboration between Genova and Wuppertal.

Schedules:

- Delays in FE chips, plus movement of opto-chips off of module, have both reduced pressure on MCC and opto-chip prototyping schedule.

Summary of DORIC-p Status

- Preliminary testing work underway at OSU and Siegen, but proceeding slowly for a variety of reasons.
- Design error with extra power-on reset circuit was found. This can be “fixed” by wire-bonding an internal test-point to VDD.
- There is a leakage problem with the nominally AC-coupled preamp input. This is the sensitive input from the PIN diode. The leakage is large enough that for any reasonable PIN bias voltage, the signal is difficult to detect. This is not understood.
- It seems that the special differential blocks in the chip core require twice the bias current that was supplied by the internal bias generator. This is not understood (such an effect should appear in decent simulations), but can be bypassed for now by supplying a larger bias from outside the chip.
- The previous two problems were seen on only 3 of the 4 die tested in Siegen.
- The delay-locked loop circuit wants to lock onto a narrow frequency range around 25 MHz. Even supplying the delay control voltage externally does not allow the chip to lock onto a 40 MHz clock at the nominal supply voltage. The narrow range and the wrong central value suggest both a design problem and a simulation/ tuning problem. Neither is understood at this time.
- Next few weeks are critical to understand problems before FE-D2 run. Do not have much confidence in the present team, but no re-inforcements are in sight.

Summary of Status of FE-H (Honeywell SOI version)

- Infrastructure work almost done (Standard Cell library, Cadence files, etc.), and last concerns about completeness of "new" Layout Rules scheme now resolved.
- Transfer agreements with collaborators "essentially" in place. Honeywell in process of shipping relevant documentation so Bonn and Marseille can begin design contributions immediately. Only CPPM will do so.
- First significant work on layout for digital readout (2x16 pixel block) indicates we can improve on several aspects of FE-D, while achieving the 300μ pixel size we want for the B-layer. This is due to smaller device size and closer packing, plus third metal layer.
- Effort on FE-H is presently significantly reduced due to activity in understanding FE-D and submitting FE-D2. This is certainly generating delay. Hope to submit GDS for engineering run by mid-Summer. Turnaround is about 20 weeks...
- Laurent should now have the necessary documentation to get started on converting the FE-D front-end design to HSOI. He is eager to get started.
- Roberto Marchesini will be returning to LBL full time in early March, which will significantly enhance our FE-H team.
- Propose to hold multi-day design workshop in Berkeley towards end of March (must be after submission of FE-D2). Should allow detailed review of status, and further progress on organization of work.

Summary of Deep Sub-micron Status

IBM situation:

- CERN people in US now discussing with IBM lawyers to search for agreement on export control issues. Many questions...
- For now, proposal is to negotiate a blanket export control agreement as part of frame contract (similar to goal for TEMIC) to allow shipment of all wafers purchased under frame contract to CERN. Hope is then that all subsequent work in other countries would be done under temporary export arrangements, with CERN as the final destination. Without minimal burden on IBM, they will drop out.
- NDA situation with France and the US not yet clear. France needs a volunteer to be a national contact (Strasbourg or CPPM). IBM still deciding on guidelines for number of US contacts, but this should be resolved soon.

Status of collaboration with RAL engineers (via Tyndel):

- Some financial support available for engineers with knowledge of IBM process to work on some “studies”. Examples could include implementing some of our circuit blocks (e.g. 2x16 digital readout) in fully static form, and verifying performance. No technical contact yet, but hopefully soon.

Within collaboration, no significant resources before the end of the year...